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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,287	11/02/2001	Je-suk Lee	SAM-0279	9042

7590 06/24/2005

Steven M. Mills
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
JELINEK, BRIAN J	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,287	LEE ET AL.	
	Examiner	Art Unit	
	Brian Jelinek	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 April 2005 and 02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

The Examiner respectfully submits a response to the amendment received on 4/29/2005 of application no. 10/000,287 filed on 11/2/2001 in which claims 1-20 are currently pending (of which claims 1-10 are currently withdrawn from consideration).

Drawings

The Examiner thanks the Applicant for correcting the drawings.

Arguments

The Applicant's arguments have been fully considered but they are not persuasive. Please refer to the following office action, which clearly sets forth the reasons for non-persuasiveness.

The Applicant argues that Terada, Roberts, and Petrick, either alone or in combination, fail to "teach or suggest that a vertical erasure signal is applied for a second time erasing a charge signal of a second horizontal line before a vertical transmission signal is applied for a second time". In response, the Examiner believes the combination of Terada and Hosier addresses the contended limitations and directs the Applicant to the rejection of claim 11 for a complete discussion.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11, 14, 16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terada et al. (U.S. Pat. No. 6,124,888), in view of Hosier et al. (U.S. Pat. No. 6,683,646).

Regarding claim 11, please note that the Examiner is interpreting the claims as follows: an image pickup method enabling, outputting, and then erasing a first horizontal line (limitations A-C); enabling and then erasing a second horizontal line (limitations D-E); and enabling and then outputting a third line (limitations F-G), presumably before erasing the third line. As such, the Examiner believes claim 11 is fairly interpreted as an image sensor that performs line skipping, wherein a first line is selected, read, and erased; a second line is selected and erased; and a third line is selected, read, and erased.

Furthermore, regarding claim 11, Terada discloses a CMD high-speed image pickup method of an image sensor including m horizontal lines (Fig. 1) with a plurality of pixels and an analog-to-digital converter (col. 11, lines 30-38), where m is an integer greater than zero, the method comprising the steps of: (a) applying a vertical selection signal (col. 13, line 15, vertical selection pulse) in response to a vertical shift clock signal (col. 10, lines 21-33), thereby enabling a first horizontal line among the m horizontal lines; (b) applying a vertical transmission signal in a first instance (col. 13, lines 26-40), thereby outputting a charge signal of the first horizontal line to the analog-

to-digital converter; and (c) applying a vertical erasure signal in a first instance, thereby erasing the charge signal of the first horizontal line (col. 13, lines 42-48).

Furthermore, Terada discloses a skip driving mode in which the vertical selection line is shifted a plurality of times during the horizontal blanking period in order to skip reading a plurality of lines (col. 10, lines 53-61). Furthermore, Terada discloses (d) shifting the vertical selection signal in response to the vertical shift clock signal, thereby enabling a second (skipped) horizontal line (col. 10, lines 53-61); (f) shifting the vertical selection signal in response to the vertical shift clock signal, thereby enabling the horizontal line following the first horizontal line (the third line which is also the next line to read) (see col. 13, lines 52-60); and (g) applying the vertical transmission signal in a second instance, thereby outputting a charge signal of the horizontal line following the first horizontal line to the analog-to-digital converter (see col. 13, lines 26-40). As such, Terada discloses enabling, outputting, and then erasing a first horizontal line (limitations A-C); enabling and then skipping a second horizontal line (limitations D-E); and enabling and then outputting a third line (limitations F-G) before erasing the third line.

Although Terada teaches the second line is skipped during the horizontal blanking period following the enabling, outputting, and erasing of the first line and before the enabling, outputting, and erasing of the third line, Terada does not disclose the charge of the skipped line is erased.

However, it is well known in the art that image sensors comprising photodiodes, such as CCD, CMD, and CMOS sensors, are prone to blooming. In particular, Hosier teaches that photodiodes are constantly outputting charge as long as light is impinging

on the photodiode resulting in blooming, which is the spread of excess charge caused by the exposure of light leaking from one photodiode to neighboring photodiodes (col. 1, lines 29-67). One of ordinary skill in the art would have enabled and then erased the charge created by the photodiode of the CMD image sensor in a skipped line during a skip reading mode for the purpose of eliminating blooming caused by the spread of excess charge leaking into neighboring pixels (col. 1, lines 29-67). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention have (e) applied the vertical erasure signal in a second instance, thereby erasing a charge signal of the second horizontal line before the vertical transmission signal is applied in a second instance to output a charge signal of a horizontal line following the first horizontal line for the purpose of eliminating blooming caused by the spread of excess charge from the skipped line leaking into neighboring pixels.

Terada further discloses the image sensor is a CMD image sensor (Fig. 7, element 103), rather than a CMOS image sensor. The Examiner is interpreting the CMD image sensor as a CMOS image sensor because a CMD sensor is "an active image sensor derived from CCD pixel technology and CMOS transistor technology".

Regarding claim 14, Terada discloses a skip driving mode in which the vertical selection line is shifted a plurality of times during the horizontal blanking period in order to skip reading a plurality of lines (col. 10, lines 53-61). As such, Terada discloses enabling, outputting, and then erasing a first horizontal line; enabling and then skipping a second horizontal line; and enabling and then outputting a third line before erasing the third line.

Although Terada teaches the second line is skipped during the horizontal blanking period following the enabling, outputting, and erasing of the first line and before the enabling, outputting, and erasing of the third line, Terada does not disclose the charge of the skipped line is erased; or the vertical erasure signal is enabled for the first and second instances during a single period of a horizontal synchronizing signal

However, it is well known in the art that image sensors comprising photodiodes, such as CCD, CMD, and CMOS sensors, are prone to blooming. In particular, Hosier teaches that photodiodes are constantly outputting charge as long as light is impinging on the photodiode resulting in blooming, which is the spread of excess charge caused by the exposure of light leaking from one photodiode to neighboring photodiodes (col. 1, lines 29-67). One of ordinary skill in the art would have enabled and then erased the charge created by the photodiode of the CMD image sensor in a skipped line during a skip reading mode for the purpose of eliminating blooming caused by the spread of excess charge leaking into neighboring pixels (col. 1, lines 29-67). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention have the vertical erasure signal enabled for the first and second instances during a single period of a horizontal synchronizing signal for the purpose of eliminating blooming caused by the spread of excess charge from the skipped line leaking into neighboring pixels.

Regarding claim 16, Terada discloses a high-speed image pickup controller of an image sensor including m horizontal lines (Fig. 1) with a plurality of pixels and an analog-to-digital converter (col. 11, lines 30-38), where m is an integer greater than zero, the controller comprising: a vertical shifter (Fig. 8, element 208, vertical scanning

circuit) for receiving a vertical selection signal (col. 13, line 15, vertical selection pulse) in response to a vertical shift clock signal (col. 10, lines 21-33) and generating an internal vertical selection signal to enable a first horizontal line or a second horizontal line among the m horizontal lines (Fig. 8, element 207, vertical selection line); a vertical erasure signal generator for receiving a system clock signal, generating a vertical erasure signal for erasing a charge signal of a horizontal line, and applying the vertical erasure signal to the first horizontal line in a first instance and applying the vertical erasure signal to a second horizontal line in a second instance (col. 13, lines 42-48; col. 13, lines 52-60); and a vertical transmission signal generator for receiving the system clock signal, generating a vertical transmission signal for outputting a charge signal of a horizontal line, and applying the vertical transmission signal to the first horizontal line in a first instance and a horizontal line following the first horizontal line in a second instance (col. 13, lines 26-40 and 52-60).

Furthermore, Terada discloses a skip driving mode in which the vertical selection line is shifted a plurality of times during the horizontal blanking period in order to skip reading a plurality of lines (col. 10, lines 53-61). As such, Terada discloses enabling, outputting, and then erasing a first horizontal line; enabling and then skipping a second horizontal line; and enabling and then outputting a third line before erasing the third line.

Although Terada teaches the second line is skipped during the horizontal blanking period following the enabling, outputting, and erasing of the first line and before the enabling, outputting, and erasing of the third line, Terada does not disclose the charge of the skipped line is erased.

However, it is well known in the art that image sensors comprising photodiodes, such as CCD, CMD, and CMOS sensors, are prone to blooming. In particular, Hosier teaches that photodiodes are constantly outputting charge as long as light is impinging on the photodiode resulting in blooming, which is the spread of excess charge caused by the exposure of light leaking from one photodiode to neighboring photodiodes (col. 1, lines 29-67). One of ordinary skill in the art would have enabled and then erased the charge created by the photodiode of the CMD image sensor in a skipped line during a skip reading mode for the purpose of eliminating blooming caused by the spread of excess charge leaking into neighboring pixels (col. 1, lines 29-67). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention have the vertical erasure signal generator apply the vertical erasure signal in the second instance before the vertical transmission signal generator applies the vertical transmission signal in the second instance to output the horizontal line following the first horizontal line for the purpose of eliminating blooming caused by the spread of excess charge from the skipped line leaking into neighboring pixels.

Terada further discloses the image sensor is a CMD image sensor (Fig. 7, element 103), rather than a CMOS image sensor. The Examiner is interpreting the CMD image sensor as a CMOS image sensor because a CMD sensor is "an active image sensor derived from CCD pixel technology and CMOS transistor technology".

Regarding claim 19, please see the rejection of claim 14.

Claims 12-13, 15, 17-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terada et al. (U.S. Pat. No. 6,124,888), in view of Hosier et al. (U.S. Pat. No. 6,683,646), and further in view of Roberts (U.S. Pat. No. 5,541,654).

Regarding claim 12, Terada discloses reading the sensor sequentially, row-by-row. Terada et al. does not disclose a first horizontal line is an arbitrary horizontal line among the m horizontal lines.

However, Roberts discloses random access of groups of image elements in the array where the first horizontal line is an arbitrary horizontal line among the m horizontal lines (Abstract, lines 8-13; Fig. 6, elements 172 and 174). One of ordinary skill in the art would have provided random access of image elements for the purpose of processing output signals indicative of only a selected part of image sensor (Abstract, lines 8-13). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the first horizontal line as arbitrary horizontal line among the m horizontal lines for the purpose of processing output signals indicative of only a selected part of image sensor.

Regarding claim 13, please see the rejection of claim 12 and further note that Roberts discloses the second horizontal line is an arbitrary horizontal line between the first horizontal line and the m-th horizontal line (Abstract; Fig. 6, elements 172 and 174).

Regarding claim 15, Terada et al. does not disclose a rate at which the vertical shift clock signal is enabled can be adjusted.

However, Roberts does disclose a rate at which the vertical shift clock signal is enabled can be adjusted (col. 10, lines 11-20). One of ordinary skill in the art would

have provided a vertical shift clock signal with an adjustable rate in order to increase frame rate (col. 10, lines 15-20). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided a vertical shift clock signal with an adjustable rate in order to increase frame rate.

Regarding claim 17, please see the rejection of claim 12.

Regarding claim 18, please see the rejection of claim 13.

Regarding claim 20, please see the rejection of claim 15.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Jelinek whose telephone number is (571) 272-7366. The examiner can normally be reached on M-F 9:00 am - 5:00 pm. If attempts to

reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached at (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Jelinek
6/22/2005

DAVID L. OMETZ
PRIMARY EXAMINER